AMENDMENTS WITH CHANGES SHOWN:

IN THE SPECIFICATION

Page 1, lines 10-27:

This application is related to U.S. Patent Application Serial No. [_____] 09/975,115, docket number CYPR-CD00182, to Warren Snyder, et al., entitled "IN-SYSTEM CHIP EMULATOR ARCHITECTURE"; and to U.S. Patent Application Serial No. [_____] 09/975,104, docket number CYPR-CD00183, to Warren Snyder, entitled "CAPTURING TEST/EMULATION AND ENABLING REAL-TIME DEBUGGING USING AN FPGA FOR IN-CIRCUIT EMULATION"; and to U.S. Patent Application Serial No. [_____] 09/975,030, docket number CYPR-CD00185, to Warren Snyder, et al., entitled "EMULATOR CHIP/BOARD ARCHITECTURE AND INTERFACE"; and to U.S. Patent Application Serial No. [_____] 09/975,338, docket number CYPR-CD00186, to Warren Snyder, et al., entitled "METHOD FOR BREAKING EXECUTION OF (TEST) CODE IN A DUT AND EMULATOR CHIP ESSENTIALLY SIMULTANEOUSLY AND HANDLING COMPLEX BREAKPOINT EVENTS". Each of these applications is filed on the same date as the present application and is hereby incorporated by reference as though disclosed fully herein. This application is also related to and claims priority benefit under 35 U.S.C. §119(e) of provisional patent application serial no. 60/243,708 filed October 26, 2000 to Snyder, et al. entitled "Advanced Programmable Microcontroller Device" which is hereby incorporated herein by reference.

Page 4, lines 18-30:

A third technique, one that is used in the [Pentium™] PENTIUM® and [Pentium Pro™] PENTIUM PRO™ series of microprocessors available from Intel Corporation, provides a special

"probe mode" of operation of the processor. When the processor is placed in this probe mode, a number of internal signals are routed to a "debug port" for use by the in-circuit emulation system. This debug port is used to permit the in-circuit emulation system to communicate with the processors at all times and, when placed in probe mode, to read otherwise inaccessible probe points within the processor. Of course, providing such a probe mode requires significant design resources to design in all such probe and debug functions and associated instruction code support into the standard processor. This, of course, increases development cost, chip complexity and chip size. Moreover, such facilities become a part of the processor design which must be carried through and updated as required as enhancements to the original design are developed.

From page 9, line 28, through page 10, line 20:

A commercial ICE system utilizing the present invention is available from Cypress [Micro Systems] MicroSystems, Inc., for the CY8C25xxx/26xxx series of microcontrollers. Detailed information regarding this commercial product is available from Cypress [Micro Systems] MicroSystems, Inc., 22027 17th Avenue SE, Suite 201, Bothell, WA 98021 [Bothell, WA] in the form of version 1.11 of "[PSoC] PSOC™ Designer: Integrated Development Environment User Guide", which is hereby incorporated by reference. ("PSOC" is a trademark of Cypress MicroSystems, Inc.) While the present invention is described in terms of an ICE system for the above exemplary microcontroller device, the invention is equally applicable to other complex circuitry including microprocessors and other circuitry that is suitable for analysis and debugging using in-circuit emulation. Moreover, the invention is not limited to the exact implementation details of the exemplary embodiment used herein for illustrative purposes.

Referring now to **FIGURE 2**, an architecture for implementation of an embodiment of an ICE system of the present invention is illustrated as system 200. In system 200, a Host computer

210 (e.g., a personal computer based on a [Pentium™] PENTIUM® class microprocessor; "PENTIUM" is a registered trademark of Intel Corporation, Santa Clara, California) is interconnected (e.g., using a standard PC interface 214 such as a parallel printer port connection, a universal serial port (USB) connection, etc.) with a base station 218. The host computer 210 generally operates to run an ICE computer program to control the emulation process and further operates in the capacity of a logic analyzer to permit a user to view information provided from the base station 218 for use in analyzing and debugging a system under test or development.

Page 11, lines 6-14:

The FPGA of the base station 218 of the current embodiment is designed to emulate the core processor functionality (microprocessor functions, Arithmetic Logic Unit functions and RAM and ROM memory functions) of the [Cypress] CY8C25xxx/26xxx series microcontrollers. The CY8C25xxx/26xxx series of microcontrollers also incorporates I/O functions and an interrupt controller as well as programmable digital and analog circuitry. This circuitry need not be modeled using the FPGA 220. Instead, the I/O read information, interrupt vectors and other information can be passed to the FPGA 220 from the microcontroller 232 over the interface 226 as will be described later.

Page 12, lines 4-16:

In the designing of a microcontroller or other complex circuit such as the microcontroller 232, it is common to implement the design using the [Verilog™] VERILOG® language (or other suitable language; "VERILOG" is a registered trademark of Gateway Design Automation Corp., Littleton, Massachusetts). Thus, it is common that the full functional design description of the

microcontroller is fully available in a software format. The base station 218 of the current embodiment is based upon the commercially available [Spartan™] SPARTAN® series of FPGAs from Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124. The [Verilog™] VERILOG description can be used as the input to the FPGA design and synthesis tools available from the FPGA manufacturer to realize the virtual microcontroller 220 (generally after timing adjustments and other debugging). Thus, design and realization of the FPGA implementation of an emulator for the microcontroller (virtual microcontroller) or other device can be readily achieved by use of the [Verilog™] VERILOG description along with circuitry to provide interfacing to the base station and the device under test (DUT).